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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,896	TAO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *9-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8 and 19-27* is/are rejected.

7)☐ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-8 and 19-27 and species 1 in the reply filed on 11/30/05 is acknowledged. The traversal is on the grounds that examination of the entire application can be made without serious burden, and both the method and product should be covered in a single search. This is not found persuasive because the product as claimed can be made by materially different processes, such as separately joining the central and peripheral substrate units to the package rather than by bonding a single substrate, and then cutting it into central and peripheral substrates. Thus, the inventions are considered distinct under MPEP §806.05(f). Since a search for the product as claimed would not encompass searching for the cutting and attachment methods appearing in the process claims, the method and product claims are not covered by a single search.

The requirement is still deemed proper and is therefore made FINAL.

Regarding the species restriction, the Applicant has elected species 1. Upon reconsideration, however, the examiner no longer considers the material of claims 1-8 and the material of claims 19-27 to define mutually exclusive concepts, as claims 19-27 relate to a non-distinct subcombination of the material of claims 1-8. Therefore, the species restriction requirement is withdrawn, and all of the Group I claims are considered to be pending.

Claims 9-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan on 5/3/03. It is noted, however, that applicant has not filed a certified copy of the application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2005/0078434 to Ho.

Ho discloses a chip package comprising: a substrate (1) having opposing top and bottom surfaces; a plurality of chip bonding pads (3) disposed on the top surface of the substrate for electrically connecting to a chip (5; see paragraph 0019); a plurality of central and peripheral contact pads (7) disposed on the bottom surface of the main substrate (see figure 2) and electrically connected to the chip bonding pads (see paragraph 0018); and a plurality of slots (4) disposed between the central and peripheral contact pads (see figure 2); and a chip (5) disposed

on the upper surface of the main substrate and electrically connected to the chip bonding pads (paragraphs 0018-0019).

5. Claims 19, 20, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,710,457 to Silverbrook.

Silverbrook discloses a chip package comprising: a main substrate (10; figures 2, 8, 13), a plurality of chip bonding pads (42) disposed on the top surface of the substrate adapted for electrically connecting to a semiconductor chip (14; see figure 9); a plurality of central (innermost rows of ball grid array in figures 2, 13) and peripheral (outermost rows of ball grid array in figures 2, 13) contact pads (18) disposed on the bottom surface of the substrate; and a plurality of slots (see figures 2-6) disposed between the central contact pads and peripheral contact pads for separating the pads; a chip disposed on the upper surface of the main substrate (14; see figures 8 and 9), and a plurality of contact pads (52) on the top surface of the main substrate (figure 9).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 6, 8, 21-24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Silverbrook in view of U.S. Patent Publication No. 2003/0146508 to Chen et al.

Silverbrook discloses a chip package comprising: a main substrate (10; figures 2, 8, 13), a plurality of chip bonding pads (42) disposed on the top surface of the substrate adapted for electrically connecting to a semiconductor chip (14; see figure 9); a plurality of central (innermost rows of ball grid array in figures 2, 13) and peripheral (outermost rows of ball grid array in figures 2, 13) contact pads (18) disposed on the bottom surface of the substrate; and a plurality of slots (see figures 2-6) disposed between the central contact pads and peripheral contact pads for separating the pads and decreasing the stress due to thermal expansion mismatches (column 1, lines 25-60) while keeping the central and peripheral substrates partially connected to each other (see figures 2-6); a chip disposed on the upper surface of the main substrate (14; see figures 8 and 9), and a plurality of contact pads (52) on the top surface of the main substrate and electrically connected to the chip contact pads (figure 9; column 3, line 40-column 4, line 20). Silverbrook further discloses a plurality of central and peripheral solder balls (20) electrically connected to the chip (see figures 7-9).

Silverbrook fails to disclose an interconnection substrate

Chen discloses a chip connection structure wherein an interconnection substrate (110, 120) is provided overlying a semiconductor chip (130), the interconnection substrate having a recessed cavity for receiving the chip (figure 2A), the interconnection substrate mechanically and electrically connecting to a lower-level wiring board through solder balls disposed on the chip (112, 161, and 162; see figure 2A), and the interconnection substrate having a plurality of contact pads (161). Chen further teaches that the interconnection substrate has a heat sink top plate (120) and a dielectric layer (110) attached to the top plate and having an opening integrated with the top plate to form the cavity.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the separated main substrate of Silverbrook with the interconnection substrate cover taught by Chen. The rationale is as follows: A person having ordinary skill in the art would have been motivated to employ the slotted substrate taught by Silverbrook as a lower-level interconnection substrate for the structure in Chen, because Silverbrook indicates that the slotted, partially separated substrate provides relief from thermal stresses, thus decreasing solder ball shearing or substrate cracking (see Silverbrook, column 1, lines 25-60; column 5, lines 1-53). Furthermore, it would be desirable for a person having ordinary skill in the art to use the interconnection substrate/cover configuration on Chen in place of a lone chip, because Chen shows that such a configuration improves heat dissipation from the semiconductor chip, improves routability between bonding wires, improves interconnection density, and decreases capacitance between neighboring signal lines (see Chen, paragraphs 0026, 0027, 0035-0037). The Examiner notes that since Chen redistributes signals from the chip region to a portion of the interconnection substrate laterally far from the chip region (see figures 2A, 3A; 161, 261, 262 are laterally spaced far from the chip), these solder balls would be connected with the "peripheral contact pads" when Chen is combined with Silverbrook.

8. Claims 1, 5, 8, 20, 21, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,720,647 to Fukuizumi in view of Ho.

Fukuizumi discloses a package comprising: an interconnection substrate (7; since plate 7 is described as carrying current from the back surface electrode of the die 5 to the substrate 1, it can be considered an interconnection substrate); a central/peripheral unitary substrate (1)

mechanically and electrically connected to the interconnection substrate (see figure 6b); a chip (5) sandwiched between the substrates, the interconnection substrate having a recessed cavity for receiving the chip (see figure 6b); a metal plate (solder plate 8) between the chip and the interconnection substrate (see figure 4a-4c); a plurality of central and peripheral solder balls (14) disposed in the central and peripheral areas of the bottom surface of the substrate and electrically connected to the chip (see figure 6b).

Fukuizumi fails to disclose that the main substrate is formed of a peripheral substrate having an opening and a central substrate disposed in the opening, wherein the peripheral substrate is separated from the central substrate, thereby decreasing stresses on the peripheral substrate due to thermal expansion mismatch.

Ho discloses providing slots (4) in the main substrate substantially surrounding the chip attach area (see figures 1 and 2), such that a peripheral substrate (portion on the outside of slots 4) and central substrate (portion in die attach region inside of slots 4) are formed, thereby decreasing stresses (paragraphs 0003, 0020, 0026). Ho further teaches that the central and peripheral substrates are partially connected (see figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Fukuizumi, such that slots are provided between the die attach area and the peripheral area of the main substrate, as suggested by Ho. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide slots separating the central, die attach portion of the main substrate from the peripheral portion, because Ho shows that the peripheral portions of a substrate are particularly sensitive to thermal expansion differences from thermal cycling processes (see Ho, paragraph 0003), and that

provision of slots between the peripheral and central portions of the substrate relieves the thermal stresses and prevents cracking of the substrate or traces (see Ho, paragraphs 0003, 0020, 0026).

Allowable Subject Matter

9. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: The primary reason for allowance is the requirement for complete separation of the central and peripheral substrates, in combination with the limitations of claim 1. The closest prior art, such as Silverbrook and Ho, as applied in the rejections supra, teaches the use of slots partially separating a central substrate from a peripheral substrate in order to relieve stress, but provide no suggestion of a complete separation. The complete separation of the central and peripheral substrates causes the additional problems of maintaining the mechanical integrity of the package, providing electrical routing between the now unconnected central and peripheral substrates, and providing mechanical attachment between the interconnection substrate and the central substrate, none of which are obviated by or in the scope of the teachings of the prior art. Thus, it is the Examiner's opinion that a person having ordinary skill in the art would not only find no motivation for completely separating the central and peripheral substrates for the type of package detailed in claim 1, but would also not feasibly know how to achieve the mechanical and

electrical attachments required for the package as described in claim 1 but having fully separated central and peripheral substrates.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Japanese Patent Publication No. 2000-100866 to Miyashita and U.S. Patent Publication No. 2003/0071353 to Noguchi disclose alternate configurations for disposing grooves in a wiring substrate for stress relief.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
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jmd

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